REMARKS

Claims 1-12 are pending in the present application. Claims 1-12 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

The abstract of the disclosure section of the specification stands objected to for various reasons stated in the Office Action. The abstract is amended above in a manner that is consistent with suggestions made in the Office Action. Entry of the amendments and removal of the objection are respectfully requested.

A number of claims stand objected to for various informalities. The claims are amended above in a manner consistent with suggestions provided in the Office Action. Entry of the amendments are respectfully requested.

Claims 1-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by Kubota. Reconsideration of this rejection and allowance of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

The present invention of amended claim 1 is directed to a fuse circuit for a semiconductor integrated circuit. The fuse circuit includes a plurality of fuses; and a plurality of transmission circuits. Each transmission circuit is coupled to a corresponding fuse of the plurality of fuses. Each transmission circuit transfers signals from an input node to an output node in response to a status of the corresponding fuse, the input and output nodes of respective adjacent transmission circuits being coupled such that the transmission circuits are arranged in series.

The present invention of amended claim 8 is directed to a fuse circuit storing information related to a semiconductor integrated circuit. The fuse circuit includes a plurality of fuses each of which has first and second terminals. The first terminal of each is connected to a power supply voltage. Each fuse stores predetermined information relevant to the semiconductor integrated circuit. The fuse circuit further includes a plurality of transmission circuits. Each transmission circuit is connected to a second terminal of a corresponding fuse of the plurality of fuses. Each transmission circuit transfers an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse. The transmission circuits are connected in series.

By providing redundant fuses associated with redundant transmission circuits in this manner, the present invention is capable of reducing fuse programming defects in the semiconductor circuit embodying the fuse circuit.

Kubota, on the other hand, is directed to an LED-array-head intensity control circuit. With reference to FIG. 2 of Kubota, the circuit 20 includes a plurality of intensity adjusting circuits 21, each including a transmission gate 24-n, transistors 23-n and 26-n, power source 8. and input terminal 25-n, configured as shown. The circuit further includes a transistor 11' that is controlled by a control circuit including amplifier 14, transistor 12 and resistor R1. In this manner, assuming transistors 23-n are of the same size, and are in an off state (as determined by a control signal applied to input terminals 25-n), the current flowing in transistor 11' is equal to the current flowing in the transistors 2 of the LED driver circuits 40 (see FIG. 3). Thus, the transistors 2 of the LED driver circuit 40 and the transistors 23-n of the intensity adjusting circuit 21 operate as a current mirror (Kubota, column 5, lines 21-29). By selectively activating some or all of the transistors 23-n, using the control signal applied to the input terminals 25-n, the voltage V_G is raised or lowered, and thus, the current applied to the transistors 2 of the LED driver circuit 40 is also varied. (Kubota, column 5, line 66 - column 6, line 32). In the embodiment of FIG. 6 of Kubota, fuses are employed for permanently programming the operation state of the

transmission gates 24-n, rather than variable programming via a command applied to the input terminals 25-n.

It is respectfully submitted that Kubota fails to teach or suggest the present invention as claimed in amended independent claims 1 and 8. In particular, it is submitted that Kubota fails to teach or suggest "the input and output nodes of respective adjacent transmission circuits being coupled such that the transmission circuits are arranged in series" (claim 1) or "wherein the transmission circuits are connected in series" (claim 8). Instead, the embodiments shown in Kubota include transmission gates 24-n, the outputs of each of which are tied to the same node B (or V_G). The transmission gates 24-n of Kubota are therefore in parallel, and not in series.

In view of the above, it is submitted that Kubota fails to anticipate the present invention as claimed in amended claims 1 and 8. Reconsideration of the rejection and allowance of claims 1 and 8 are therefore respectfully requested. With regard to the various dependent claims 2-7 and 9-12, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the specification:

The abstract of the invention section of the specification is amended above as follows:

(Amended) In a fuse circuit including programmable fuses in a semiconductor integrated circuit, the fuses store specific information related to the semiconductor integrated circuit, such as redundancy information, wafer lot number, die lot number, and die position on the wafer, etc. [While a conventional semiconductor integrated circuit utilizes a single fuse for storing one bit of specific information, the] The fuse circuit [in the present invention] utilizes a plurality of fuses for storing identical bit information. Consequently, in the case where a fuse has not been cut out correctly, the fuse circuit of the present invention can reduce programming defects, whereby defect generation rates are remarkably decreased.

In the Claims:

Claims 1-12 are amended above as follows:

1. (Amended) A fuse circuit for a semiconductor integrated circuit, comprising:

a plurality of fuses; and

a plurality of transmission circuits, each transmission circuit being coupled to a corresponding fuse of the plurality of fuses; each transmission circuit for transferring signals from an input node to an output node in response to a status of the corresponding fuse [fuses], the input and output nodes of respective adjacent transmission circuits being coupled such that the transmission circuits are arranged in series.

2. (Amended) The fuse circuit of claim 1, wherein each fuse in the plurality of fuses has [have] an identical fusing status.

3. (Amended) The fuse circuit of claim 1, wherein each of the fuses includes first and second terminals, [two ends in which one] the first terminal of each being [end is] connected to a first power supply voltage.

4. (Amended) The fuse circuit of claim 3, wherein [the transmission circuits correspond to the fuses,] each of the transmission circuits comprises [comprising]:

a transmission gate having an input terminal coupled to a corresponding input node, an output terminal coupled to a corresponding output node, and a primary control terminal connected to the second terminal [other end] of [a] the corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the second terminal [other end] of the corresponding fuse and the primary control terminal, and having an output terminal connected to the secondary control terminal.

5. (Amended) The fuse circuit of claim 4, wherein the transmission gate includes:

a first conductive transistor having a first electrode connected to the input terminal, a control electrode connected to the second terminal [other end] of the corresponding fuse, and a second electrode connected to the output terminal; and

a second conductive transistor having a second electrode connected to the input terminal, a control electrode connected to the output terminal of the inverter, and a first electrode connected to the output terminal.

6. (Amended) The fuse circuit of claim 4, wherein the power supply voltage is applied to the input terminal of a first in the series of the plurality of the transmission gates.

7. (Amended) The fuse circuit of claim 5, wherein each of the transmission circuits further comprises a resistor [where one end] having a first terminal that is connected to the control electrode of the first conductive transistor and to the input terminal of the inverter,

and [the other end] having a second terminal that is connected to a second [the] power supply voltage.

8. (Amended) A fuse circuit storing information related to a semiconductor integrated circuit, comprising;

a plurality of fuses each of which has first and second terminals, the first terminal of each being [two ends in which one end is] connected to a power supply voltage, the fuses each storing predetermined information relevant to the semiconductor integrated circuit; and

a plurality of transmission circuits, each transmission circuit connected to [one of a respective other ends of the] a second terminal of a corresponding fuse of the plurality of fuses, each transmission circuit [for] transferring an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse [fuses],

wherein the transmission circuits are connected in series.

9. (Amended) The fuse circuit of claim 8, wherein the plurality of fuses in combination store one-bit of the predetermined information relevant to the semiconductor integrated circuit.

10. (Amended) The fuse circuit of claim 8, wherein each of the transmission circuits comprises:

a transmission gate having an input terminal, an output terminal, a primary control terminal connected to the second terminal [other end] of a corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the second terminal [other end] of the corresponding fuse and the primary control terminal, and an output terminal connected to the secondary control terminal.

11. (Amended) The fuse circuit of claim 10, wherein the transmission gate includes:

a NMOS transistor having a drain connected to the input terminal, a gate connected to the [other end] second terminal of the corresponding fuse, and a source connected to the output terminal; and

a PMOS transistor having a source connected to the input terminal, a gate connected to the output terminal of the inverter, and a drain connected to the output terminal.

12. (Amended) The fuse circuit of claim 11, wherein each of the transmission circuits [circuit] further comprises a resistor having a first terminal that [where one end] is connected to the control electrode of the NMOS transistor and the input terminal of the inverter, and having a second terminal that [the other end] is connected to the power supply voltage.